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Computing with nanowires: A neural architecture

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Collaborators

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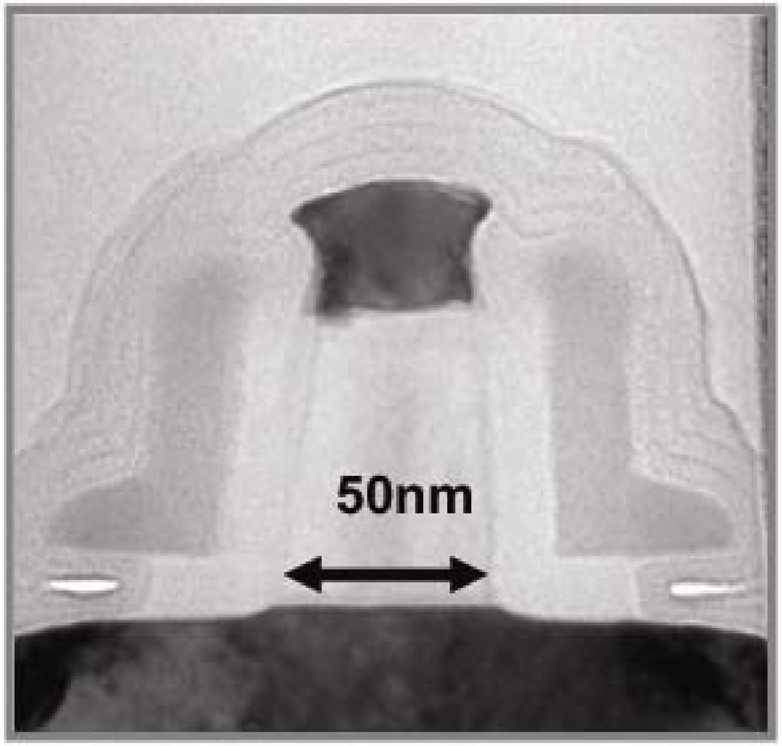
- Frazer Williams – Univ. Nebraska
- Kang Wang – UCLA
- Pinaki Mazumder – Univ. Michigan

Current students

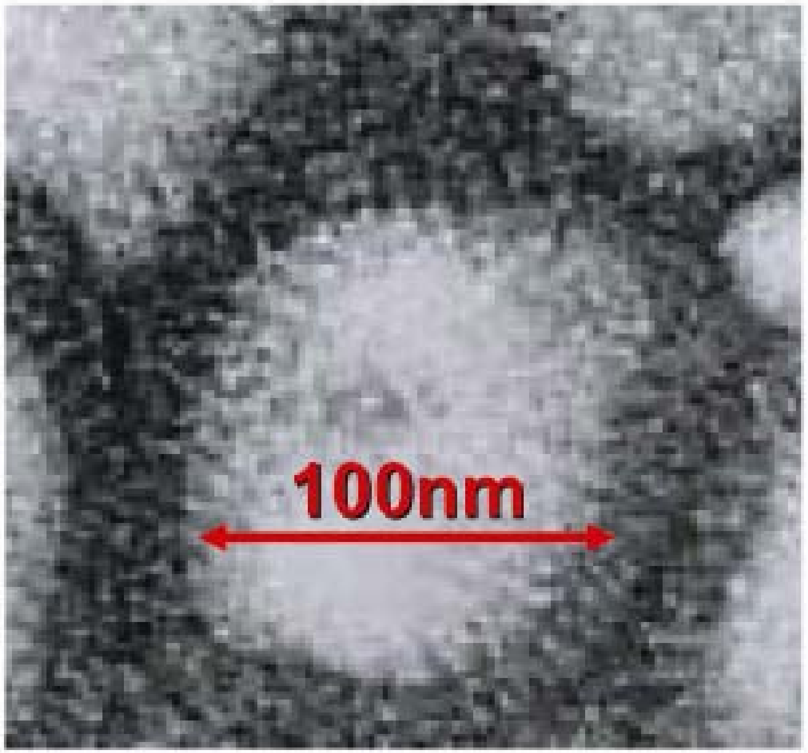
- Sandipan Pramanik
- Sridhar Patibandla

The workhorse of modern electronics has been the celebrated MOSFET….

Production Transistors Smaller Than Virus



Si transistor in the 90nm logic technology node: currently in production

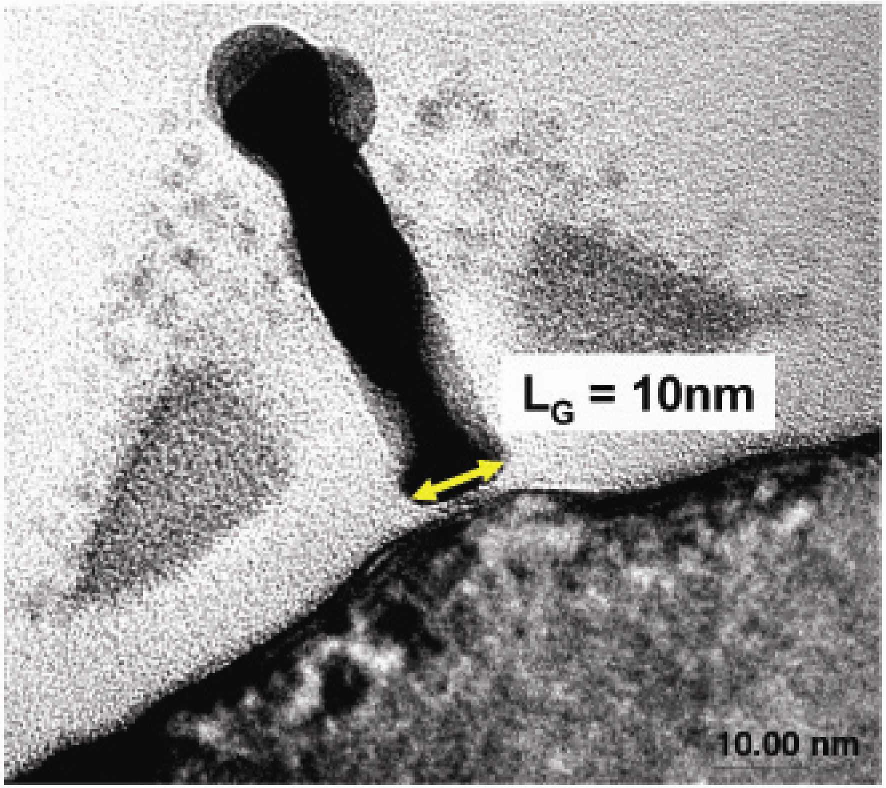


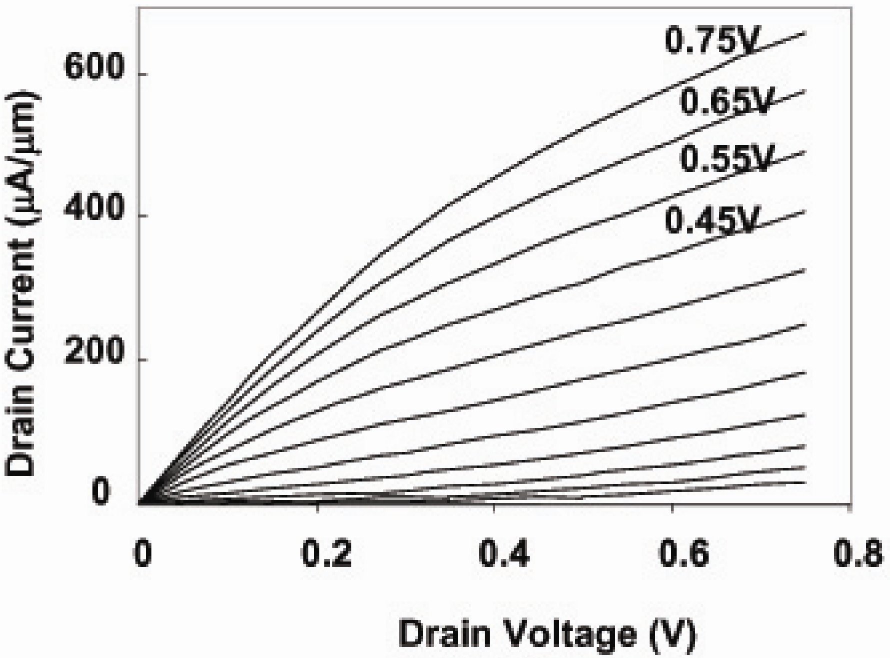
Influenza virus

Source: CDC

Courtesy: Suman Datta, Intel Corp.

Experimental 10nm Si MOS Transistor



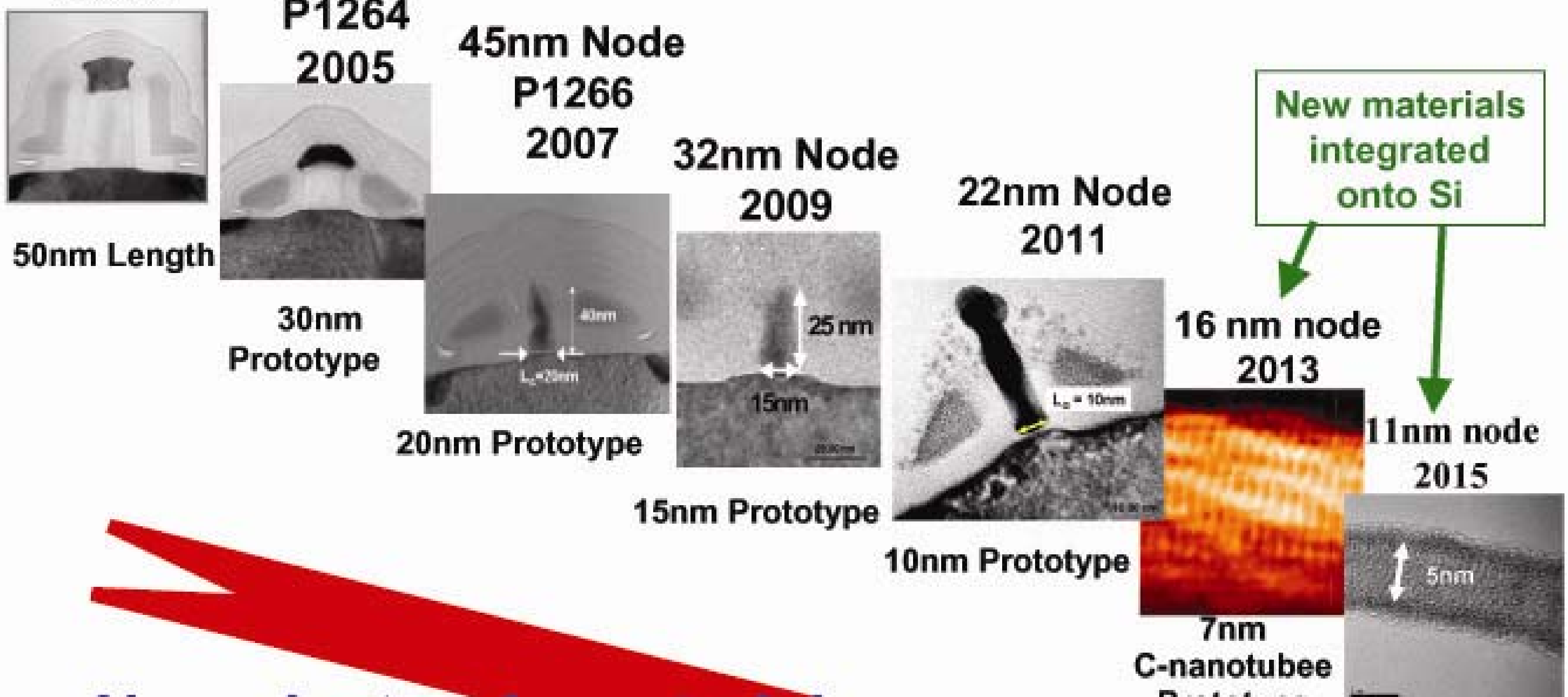


- 10nm transistor still behaves like a transistor !

But barely… Gain < 1

Courtesy: Suman Datta, Intel Corp.

Silicon Transistor Scaling and Moore's Law will Continue through 2015 ……



New electronic materials, nano-technologies and nano-architecture introduced along the way

R.Chau, S. Datta, Intel, Nov20 2003

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Prognosis

- Silicon CMOS – perhaps augmented by CNT devices – will probably continue till 2015
- …But cost will likely balloon

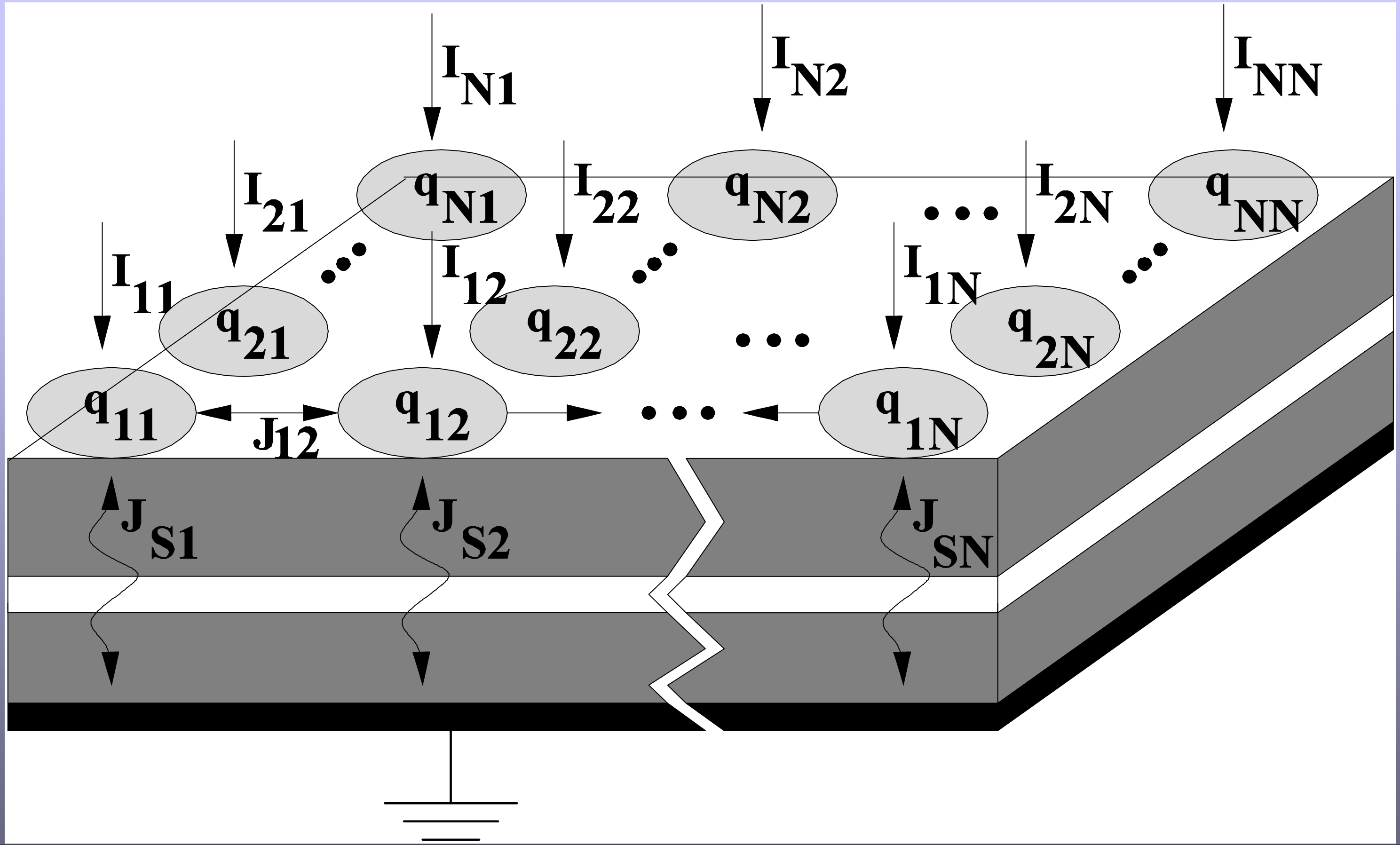
Are there alternates?

- Discard the transistor paradigm..
- “Compute” with 2 terminal nanodevices such as quantum wires and quantum dots which are incomparably easier to fabricate
- 2-terminal devices will not have “gain” or “isolation between input and output terminals” so that Boolean logic will not appropriate
- Adopt radically different architectures… e.g. neural or CA
- Specially appropriate for nanoelectronics… Nanodevices are rather irreproducible and error-prone. Neural architectures work on the basis of collective computational models. Therefore, naturally fault-tolerant.

First proposed in 1996:
V. P. Roychowdhury, D. B. Janes and S. Bandyopadhyay, IEEE T-ED, 43, 1688 (1996)

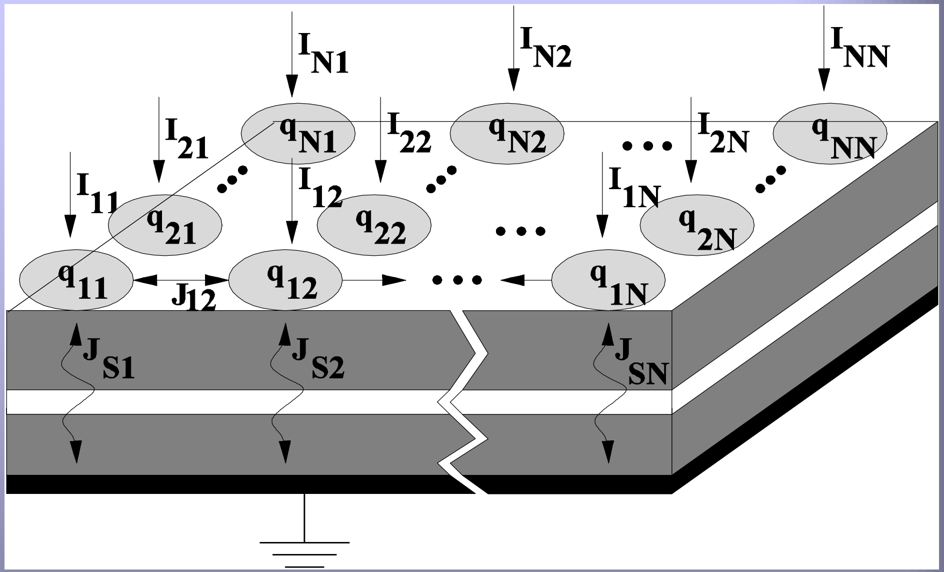
Review
S. Bandyopadhyay, V. P. Roychowdhury and D. B. Janes, "Chemically self assembled nanoelectronic computing networks" in Quantum Based Devices and Systems, Eds. M. Stroscio and M. Dutta, World Scientific, Singapore, (1998), Chapter 1.

A Self Assembled Nano-electronic Architecture: QNN



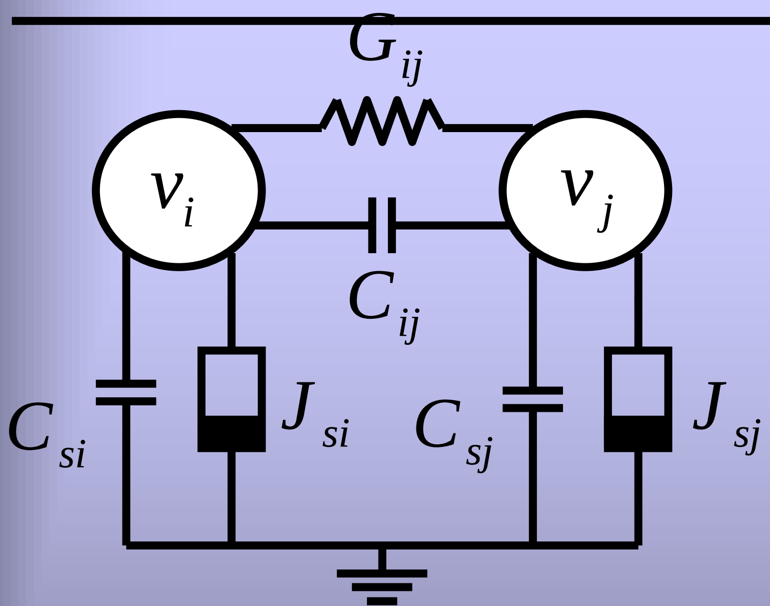
Essential ingredients

- A 2-D array of nanoparticles on a non-ohmic substrate whose I-V characteristic has a non-monotonic non-linearity, e.g. an NDR.
- Each nanoparticle is resistively and capacitively linked to its nearest neighbor nanoparticles

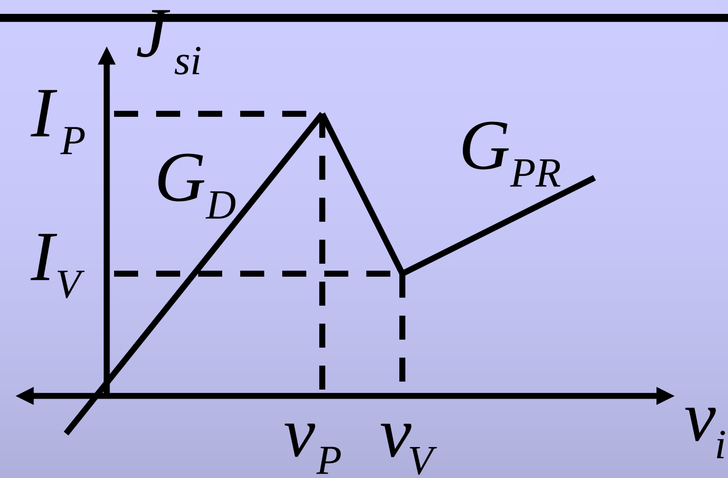


A “bottom up” approach to electronics

VCU Quantum Dot Network Circuit Model

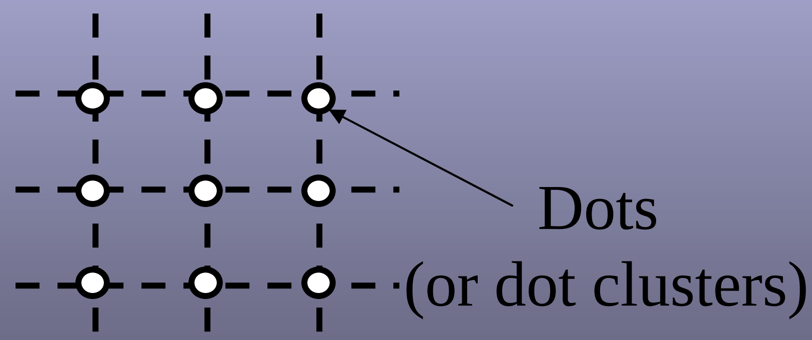


Dot pair circuit model



NDR piecewise model

Network Connectivity (Top view):



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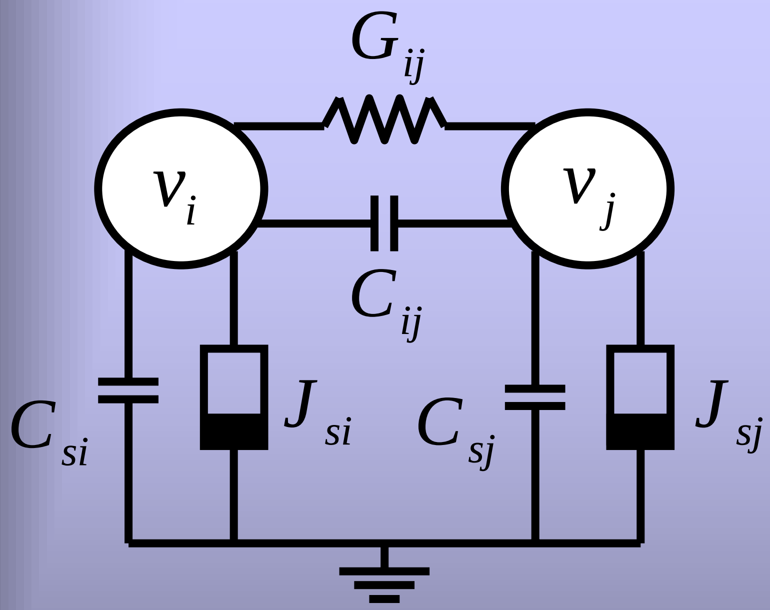
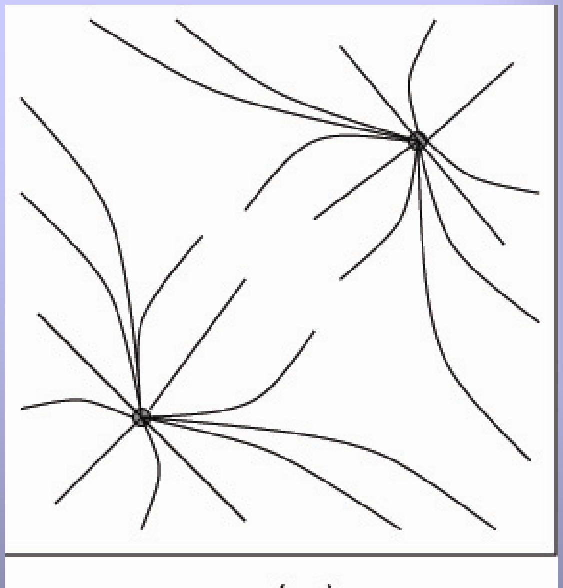
What can this “bottom up” architecture do?

- Given the NDR characteristic, this architecture generates
  - The STM model of neural networks (associative memory)
  - Can do image processing with an unprecedented density of 10^{10} pixels/cm^2
  - Can solve combinatorial optimization problems (exploiting single electron charging effects), e.g. the traveling salesman problem
  - Boolean logic circuits (NAND and NOR gates). *V. P. Roychowdhury, D. B. Janes and S. Bandyopadhyay, Proc. IEEE, 85, 574 (1997).*
  - Mimics biological systems… replicates the Fitzhugh-Nagumo model of impulse propagation along nerve cell membranes
  - Propagates trigger waves, etc.

Associative memory



V_2



(a)

V_1

$$C_{s1}dV_1/dt + J_{s1}(V_1) + C_{12}d(V_2-V_1)/dt + G_{12}(V_2-V_1) = 0$$

$$C_{s2}dV_2/dt + J_{s2}(V_2) + C_{12}d(V_1-V_2)/dt + G_{12}(V_1-V_2) = 0$$

Merits

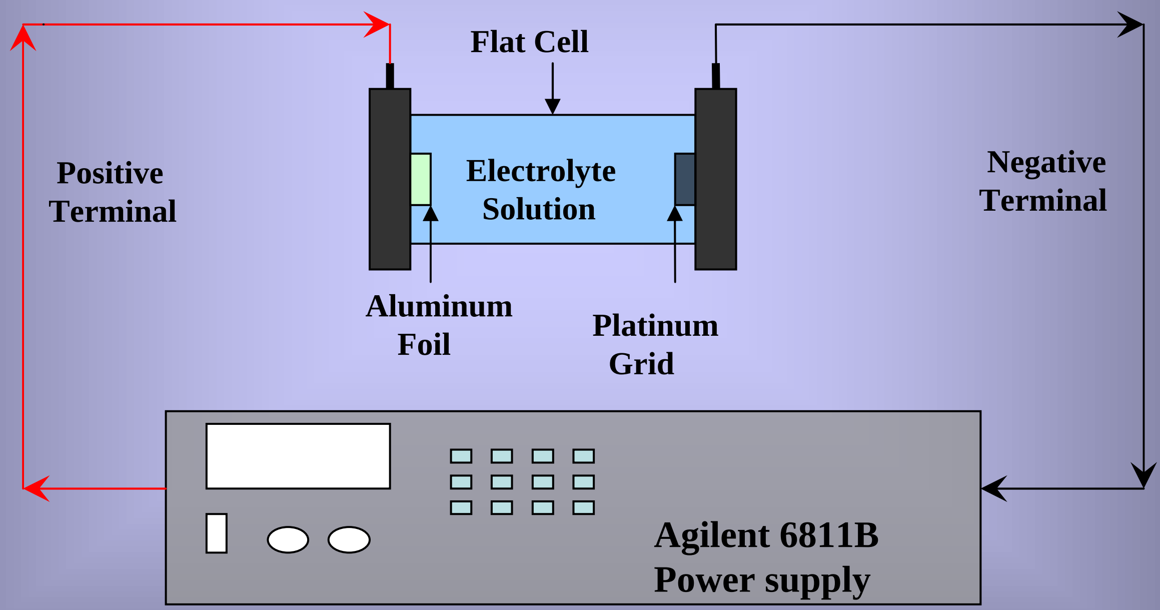
- Applications are realized all by hardware.. Almost no software involved. Hence special purpose architectures and blazing fast.
- Very little power consumption.
  - Pentium IV dissipates ~ 100 W/cm^2 with a device density < 10^9/cm^2
  - QNN dissipates ~ 1-10 W/cm^2 with a device density of 10^{11}/cm^2

Fabrication

M ediaeval

B eaker

E lectrochemistry


Flat Cell
Positive Terminal
Electrolyte Solution
Negative Terminal
Aluminum Foil
Platinum Grid
Agilent 6811B Power supply

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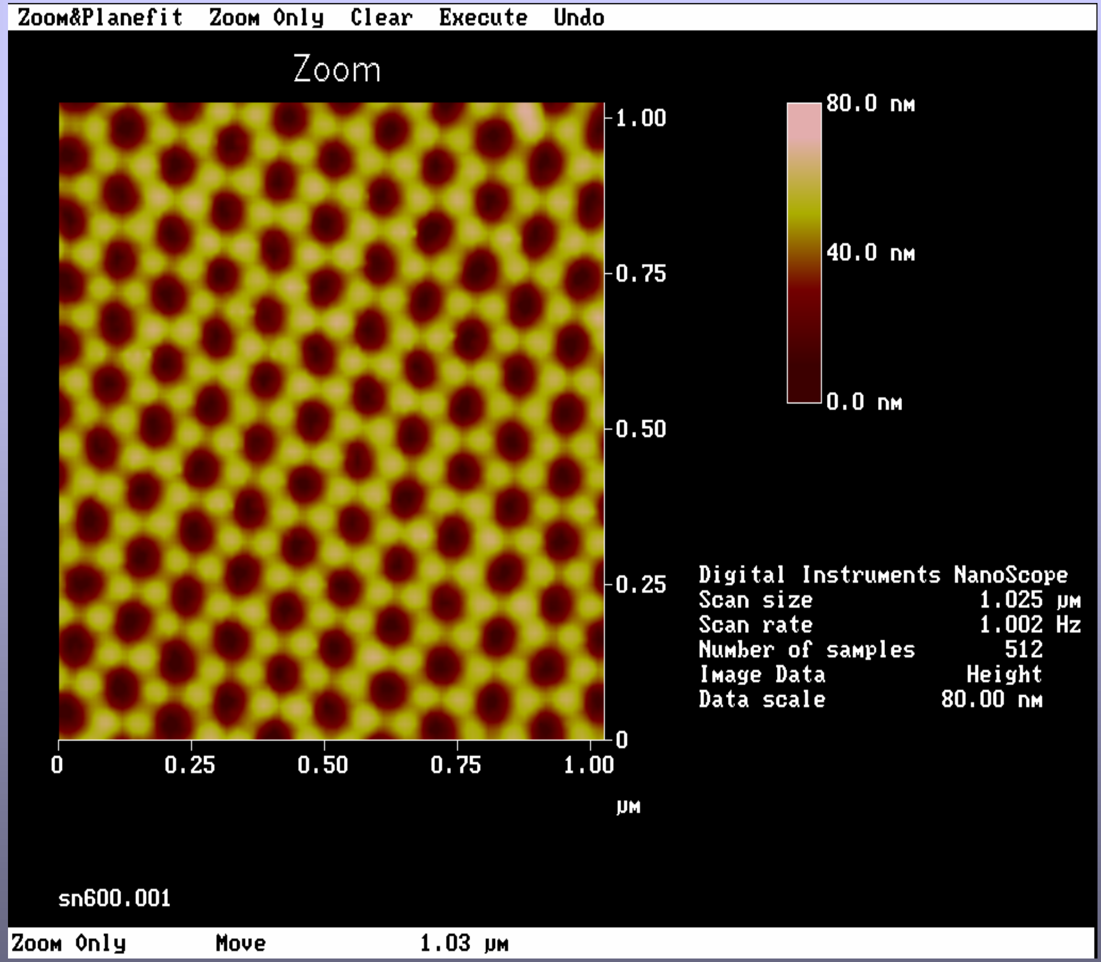
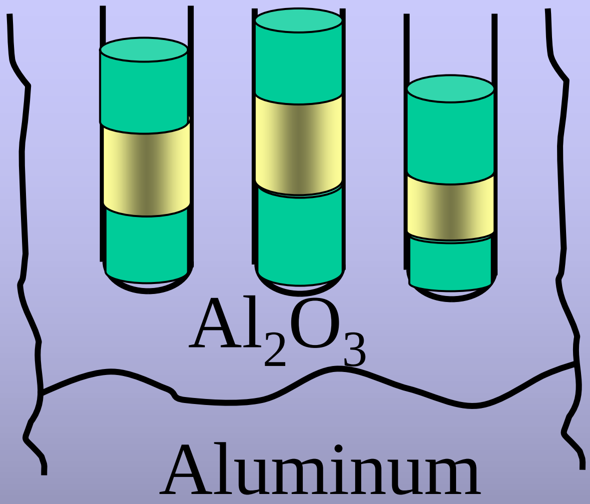
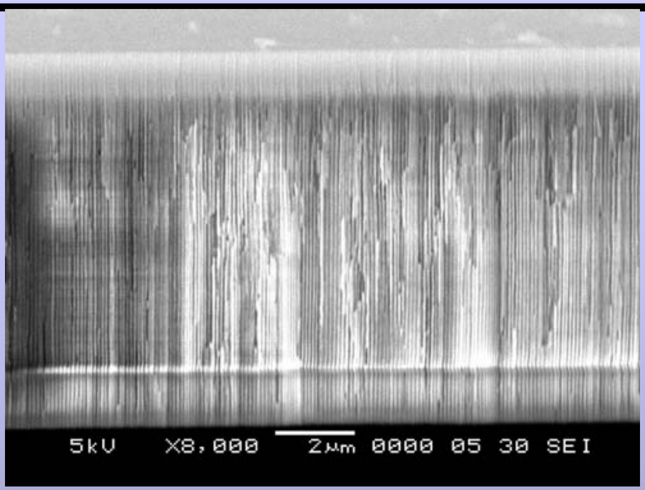
AFM Micrograph of 50-nm linked metal particles on NDR conductors

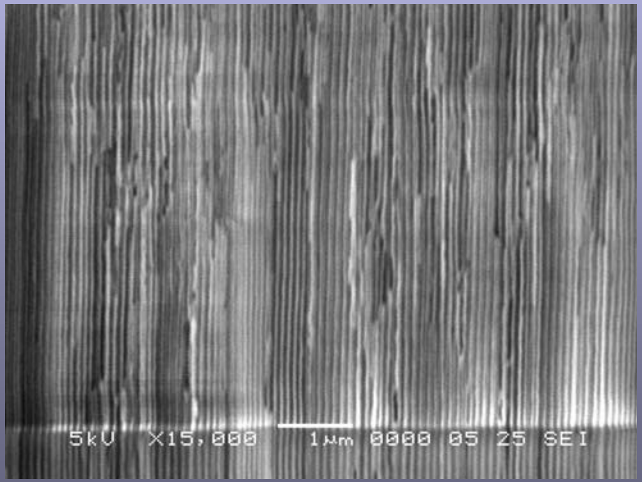


Quantum Device Laboratory

Filling up the pores







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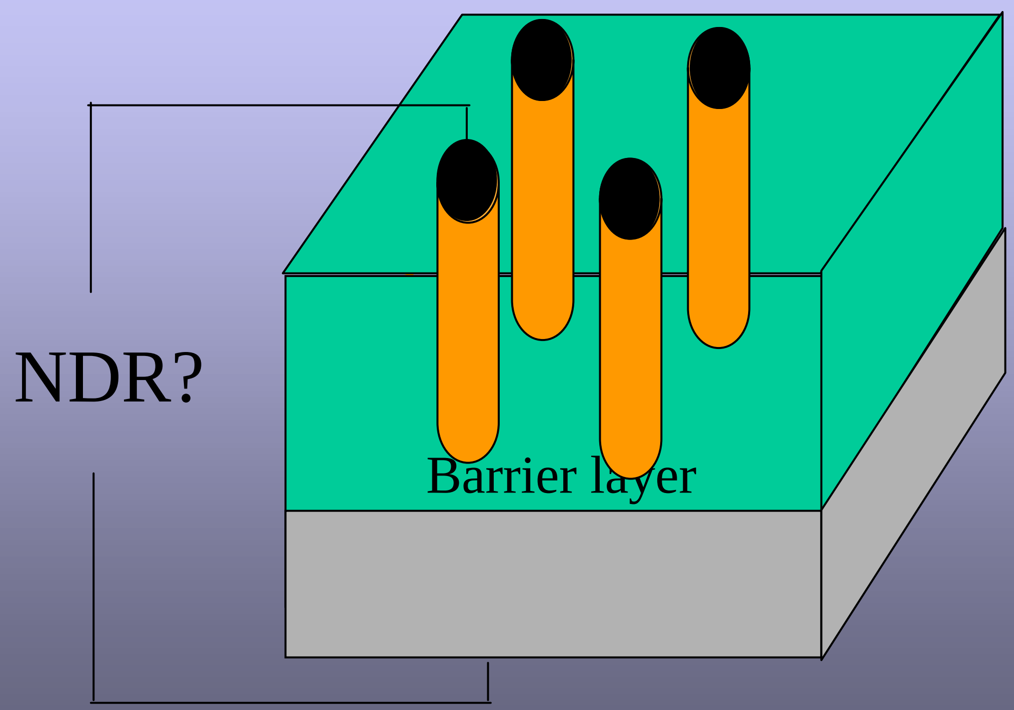
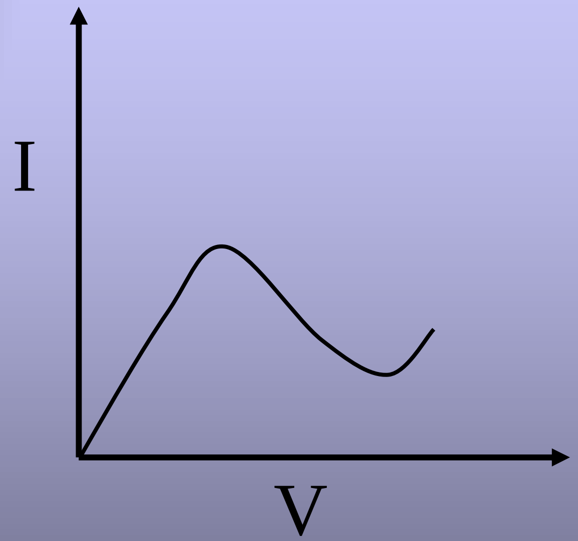
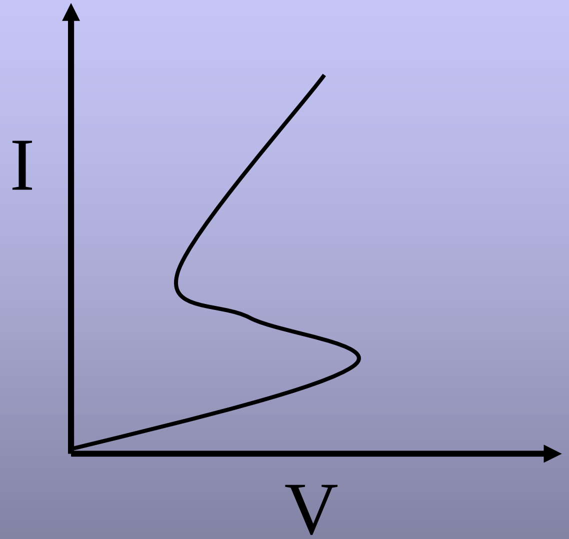
Self Assembled Network



Two types of NDR

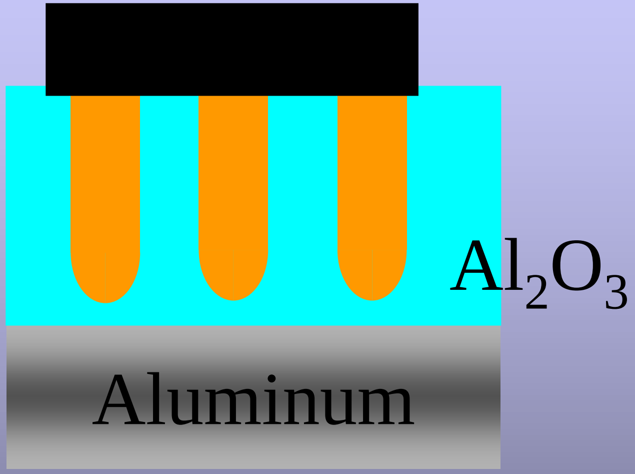


N-type



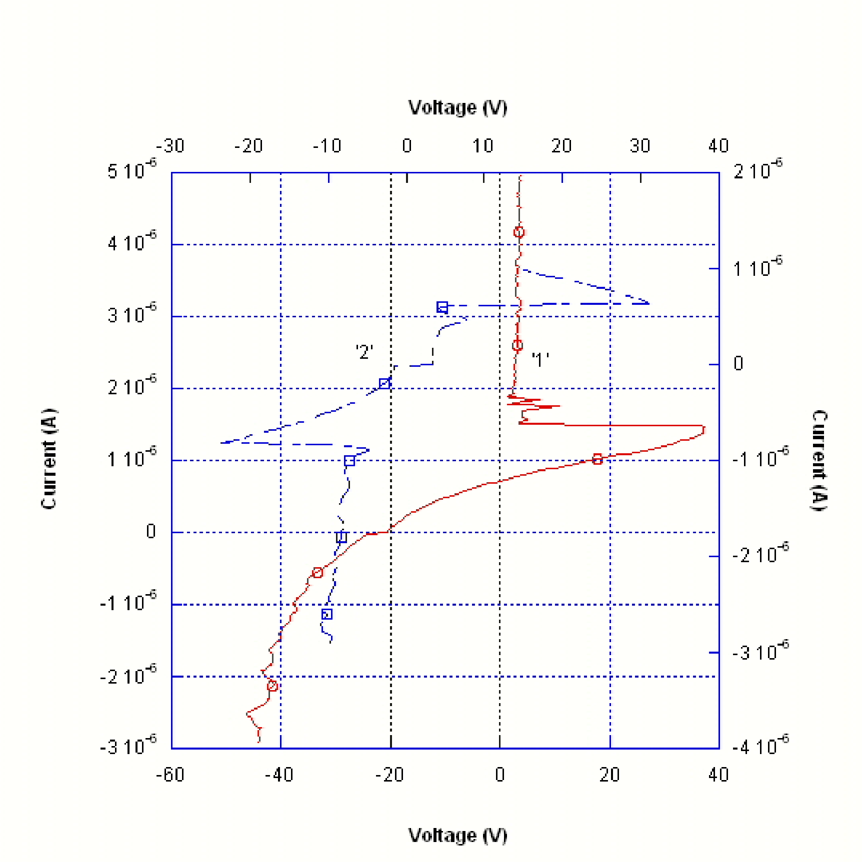
S-type

Nanoscale MIS diodes



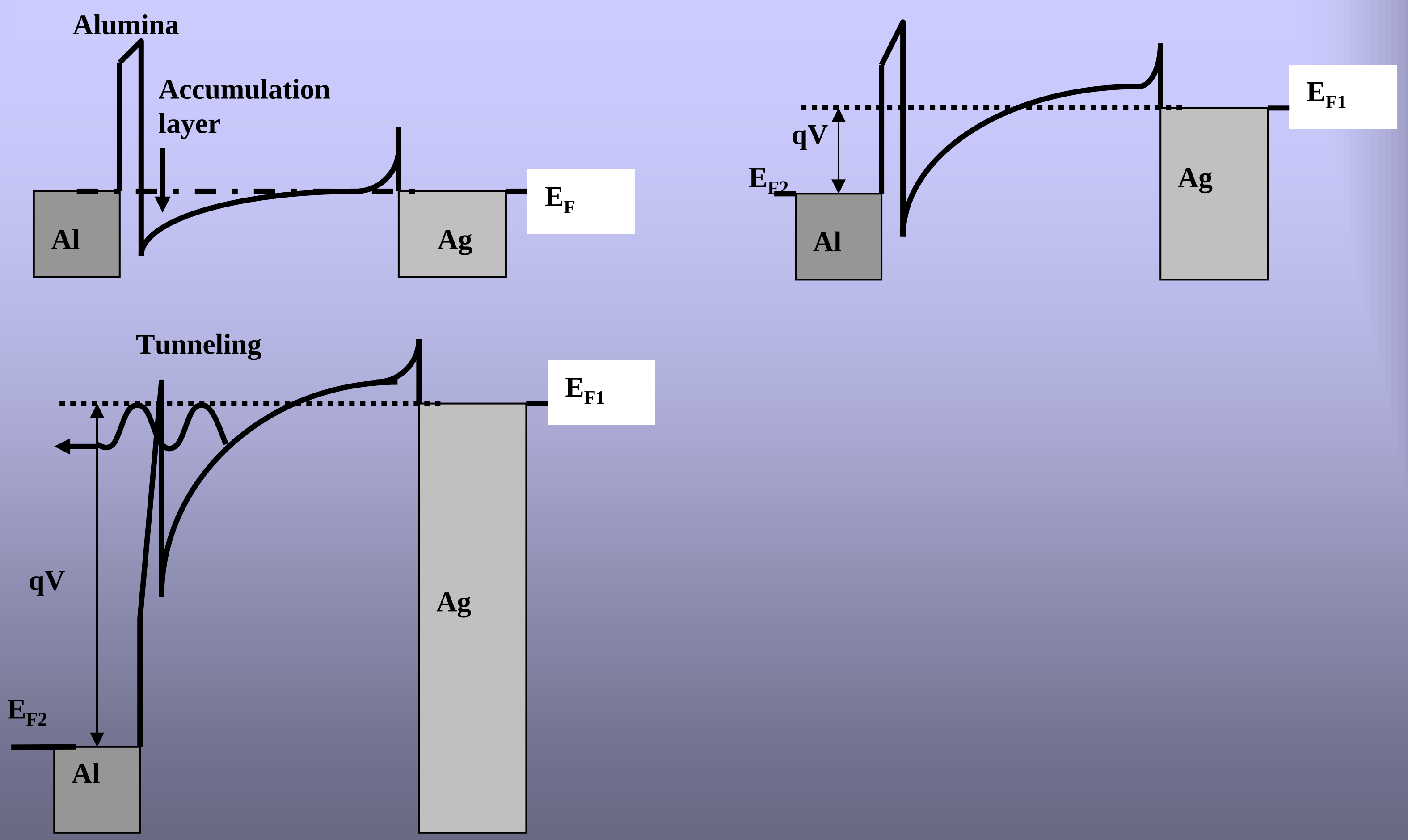
- MIS diode
- Has a thyristor type characteristic with an S-type NDR

S-type NDR



Peak to valley ratio = 19:1at 300 K

Origin of S-type non-linearity



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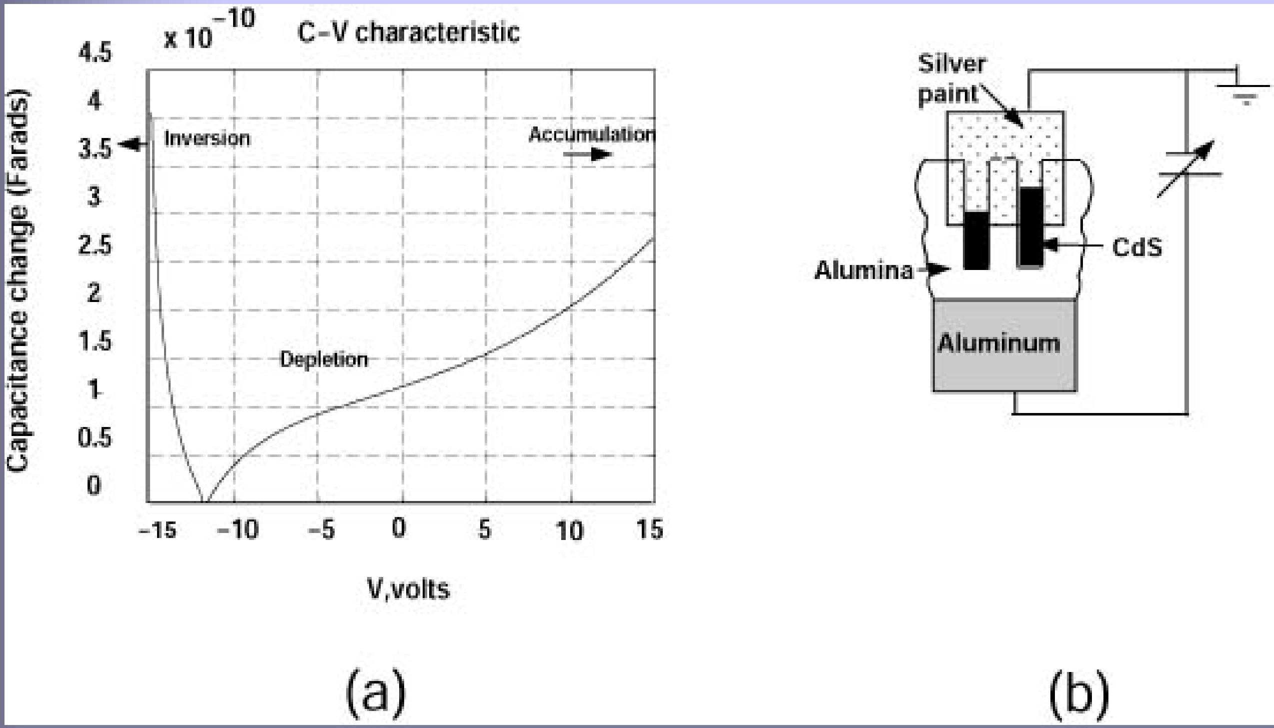
Circuit parameters

- So we have the NDR and can measure the peak current and the “slopes”
- What about
  - C_{si}
  - G_{ij}
  - C_{ij}

C-V characteristics



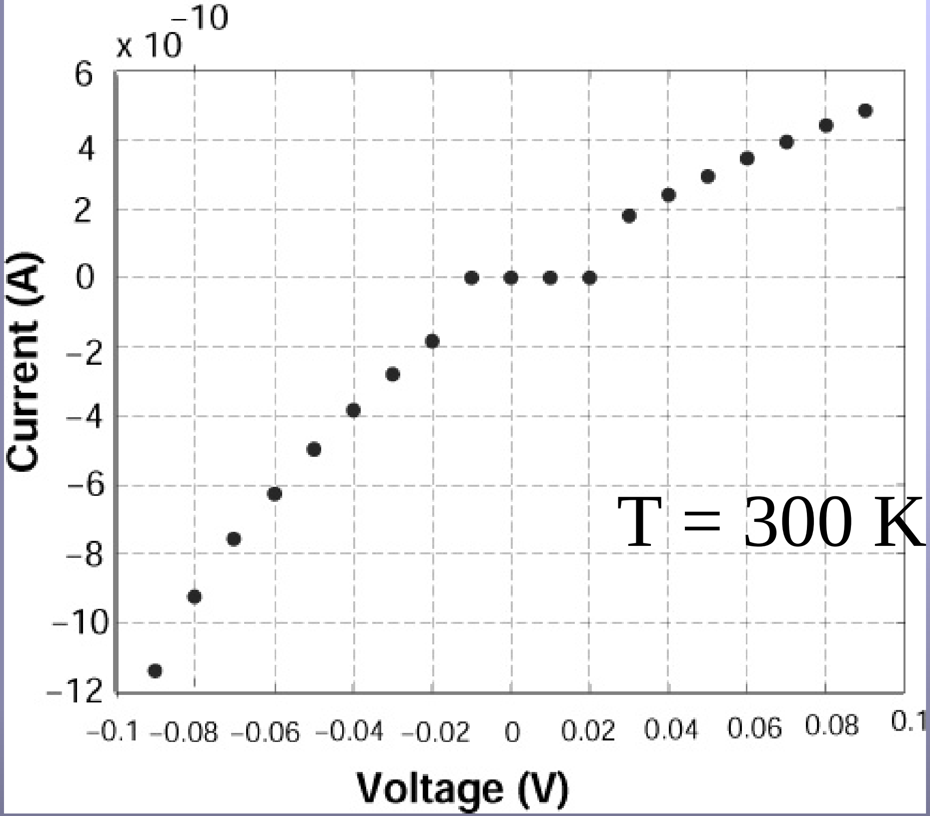
Contact area is 1 mm^2

Wire density is 10^{11}cm^{-2}, so that 10^9 wires are contacted

Capacitance per wire is 0.5 aF

N. Kouklin and S. Bandyopadhyay
Technical Digest of ISCS, IEEE Press, pp. 303-308 (2000);
See also, N. Kouklin, L. Menon and S. Bandyopadhyay, APL, 80, 1649 (2002)

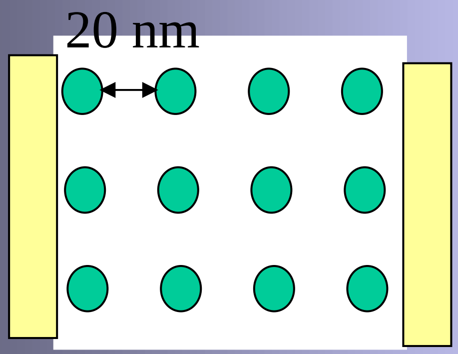
Current voltage characteristics of few dots



Room temperature
Coulomb blockade

N. Kouklin, L. Menon and S. Bandyopadhyay
APL, <u>80</u>, 1649 (2002).

Characterization of the linking matrix



Measured resistivity of alumina = 160 kΩ-cm

See, N. Kouklin, et. al. APL, 76, 460 (2000).

In collaboration with Kurchatov Institute, Moscow, Russia

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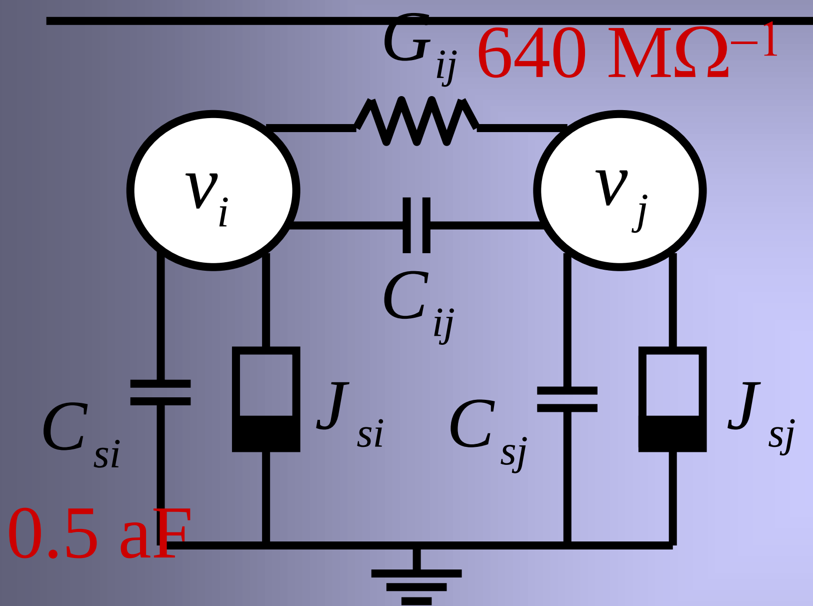

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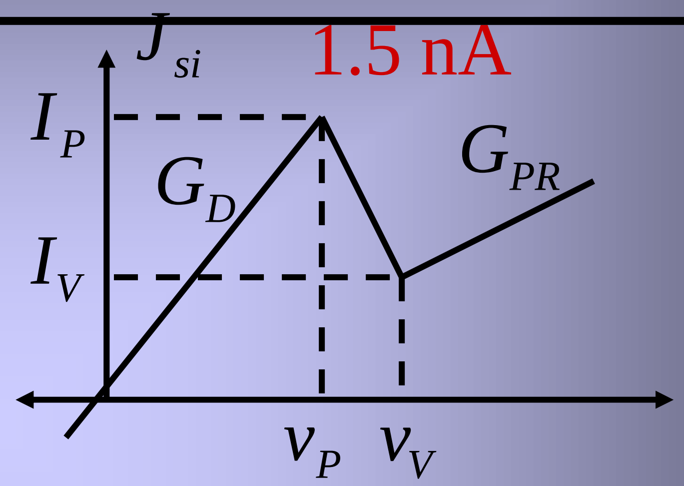
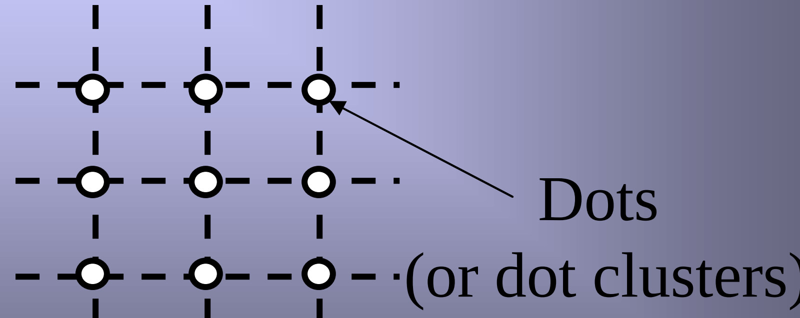


NDR piecewise model

Network Connectivity (Top view):



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Circuit parameters based on measured values

- Single dot : $R_{inter\text{-}dot}$ = 640 MΩ
- Single dot: $C_{inter\text{-}dot}$ = 5 aF
- Single dot: $C_{substrate}$ = 0.5 aF
- Single dot: Peak current = 1.5 nA

- Superdot (1 pixel = 6400 dots):
  $R_{inter\text{-}superdot}$ = 8 MΩ
- Superdot: $C_{inter\text{-}superdot}$ = 4 fF
- Superdot: $C_{substrate}$ = 3.2 fF
- Superdot: Peak current = 0.1 μA

Since a pixel edge should be 10 times the wavelength of light, a typical pixel will contain about 6400 dots. A cluster of 6400 dots is called a “superdot”

A Quantum Dot Image Processor: Edge detection enhancement

Very fast response time of < 1 nsec

K. Karahaliloglu, S. Balkir, S. Pramanik and S. Bandyopadhyay, IEEE TED, 50, 1610 (2003)

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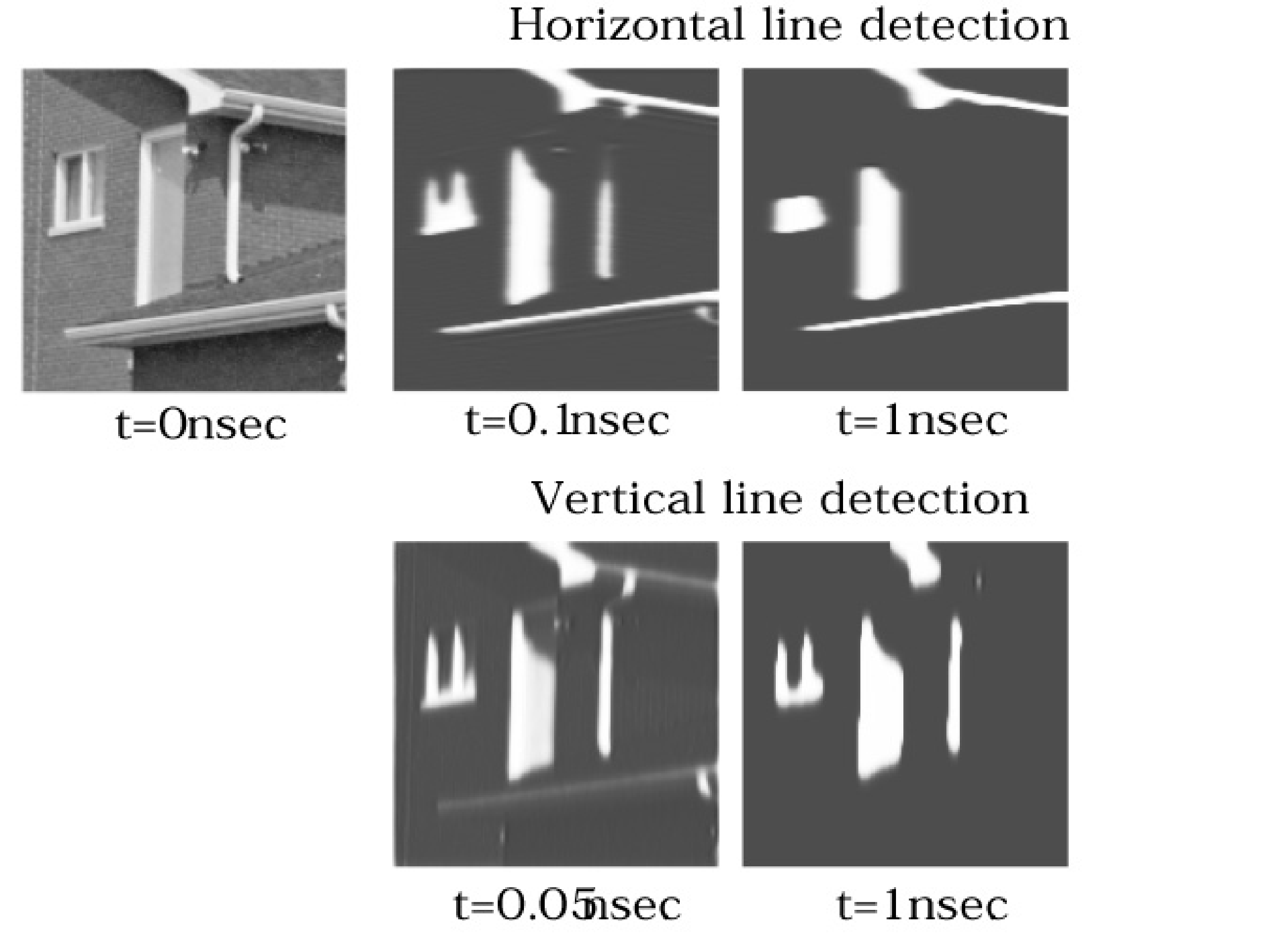
A Quantum Dot Image Processor: Horizontal/vertical line detection



Very fast response time of 1 nsec

K. Karahaliloglu, S. Balkir, S. Pramanik and S. Bandyopadhyay, IEEE T-ED, 50, 1610 (2003)

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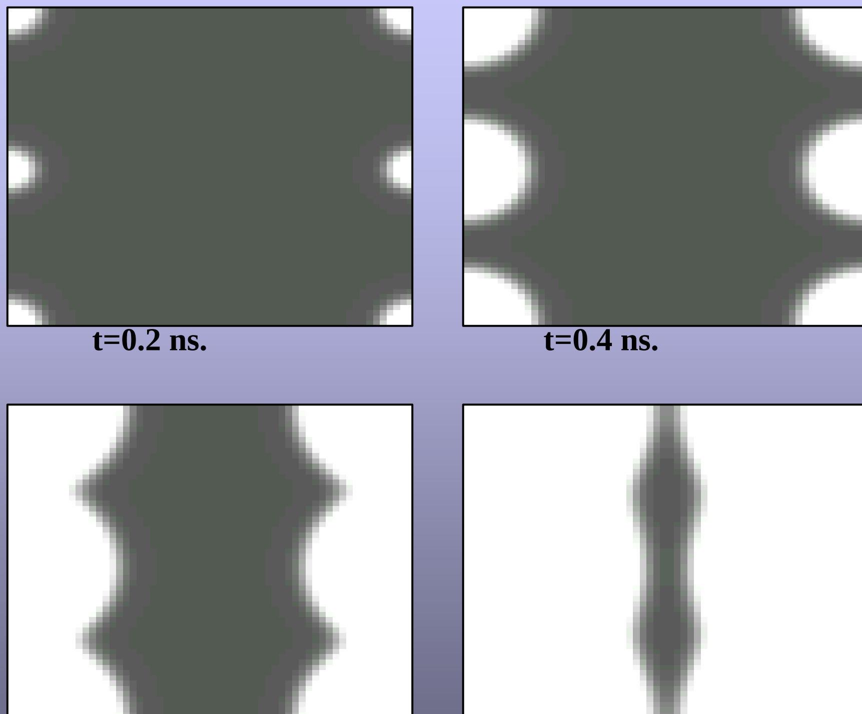
Propagation of trigger waves

Auto waves (1-Layer CNN)

Trigger Wave Formation



t=0.2 ns. **t=0.4 ns.**

t=0.6 ns. **t=0.9 ns.**

K. Karahaliloglu and S. Balkir, “Nanostructure Array of Coupled RTDs as Cellular Neural Networks,” ***International Journal of Circuit Theory and Applications***, Vol. 31, pp. 571-589, 2003.

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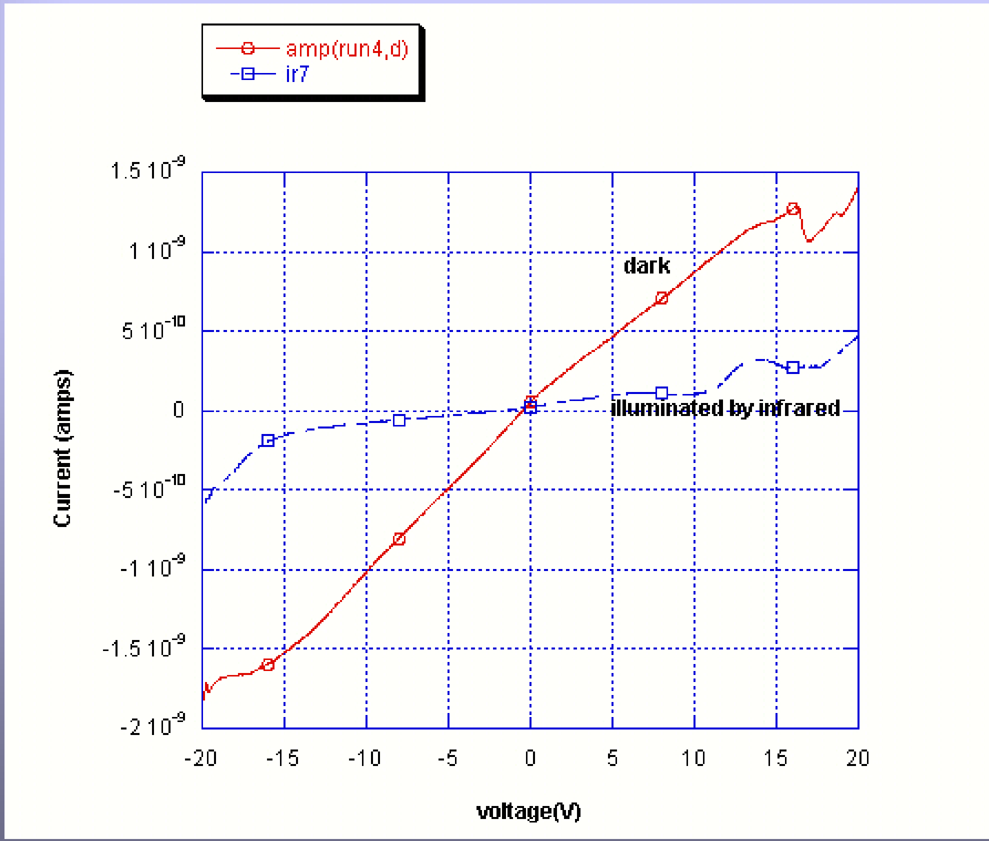
Modifying NDR characteristics with infrared illumination



Modifying the NDR with illumination.. *Programming with light*

S. Bandyopadhyay, K. Karahaliloglu, S. Balkir, S. Pramanik Proc. IEE –CDS, 152, 85 (2005)

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Conclusion

- Locally interconnected.. Only nearest neighbor connection
- Massively fault tolerant (simulation shows that architecture can work even if 30% of the devices fail)
- Reproducibility is not necessary. Architecture is based on collective computational models, where the cooperative interactions of many devices, acting in unison, matters. No single device is critical. We do not have to strive against stochasticity
- Switching speed is 0.1 psec
- Power dissipation is 0.01 nW/device
- Integration density achievable with self assembly techniques approaches 1 trillion devices per sq-cm
- Far ahead of the SIA International Technology Roadmap for Semiconductors for the year 2015